REMARKS

Claims 1, 4-6, 8-10 and 14-20 remain pending in the present application.

Claims 1, 4-6, 8-10 and 14-20 in view of Igari and Admitted Prior Art

Claims 1, 8, 16 and 17 were rejected under 35 USC 102(b) as allegedly being anticipated by Japanese document No. JP404026226A ("Igari"); and claims 4-6, 9, 10, 14, 15 and 18-20 were rejected under 35 USC 103(a) as allegedly being obvious over Igari in view of applicant's admitted prior art (AAPA). The Applicant respectfully traverses the rejections.

Claims 1, 4-6 and 8-10, 14 and 15 recite **only ONE diode voltage drop** switchably connected between each row conductor and each column conductor. Claims 16-20 recite monitoring each of a plurality of column conductors for a given voltage drop including a **SINGLE diode voltage drop** corresponding to a closed switch to a driven one of said plurality of row conductors, while one of said plurality of row conductors is being driven with a predetermined row voltage level, and monitoring each of the plurality of row conductors for a given voltage drop including a **SINGLE diode voltage drop** corresponding to a closed switch to a driven one of the column conductors, while one of the plurality of column conductors is being driven with the predetermined column voltage level.

The Examiner cites Igari for allegedly generally disclosing row conductors and column conductors as recited in the claims. (Office Action at 3) The Examiner admits that Igari fails to disclose the use of momentary and persistent type switching elements, but alleges that the background of the present specification discloses that such switching elements are conventional. (Office Action at 3).

Igari teaches, in Fig. 2, what appears to be a switch matrix including 18 switches using only 3 columns and 3 rows. According to Igari, diodes are **stacked** between GROUND and the column drivers. By 'stacking' we refer to the **series** connection of multiple diodes to a particular column driver.

For example, when column I/O3 is driven in Fig. 2 of Igari, the voltage level of the upper left hand switch SW1 will be approximately **THREE** (3) diode voltage drops (e.g., 2.1 volts). The same is true for all columns, and will get worse (i.e., the voltage drop will increase) as the switch matrix gets larger.

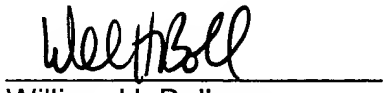
According to the present invention, only ONE diode is switchably placed between any column and any row, so that the measured voltage when a switch is activated is a much stronger 0.7 volts. Measuring a 0.7 volts as a LOW is much more reliable, and provides much more tolerance than does the measurement of 2.1 volts as a LOW as taught by the **stacked** use of diodes disclosed by Igari.

For at least all the above reasons, claims 1, 4-6, 8-10 and 14-20 are patentable over the prior art of record. It is therefore respectfully requested that the rejections be withdrawn.

Conclusion

All objections and rejections having been mooted by the cancellation of prior claims, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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